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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,547	04/19/2004	Lukas P.P.P. van Ginneken	SYNP 1006-0	3884

36454 7590 03/03/2010

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
03/03/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,547	VAN GINNEKEN, LUKAS P.P.P.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5 and 7-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5 and 7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/828,547 and response filed on 12/15/09. Claims 2, 5 and 7-18 remain pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The amended claim limitation "delay values...as a function of delay to be provided by the corresponding cells and delay to be provided by loads on the corresponding cells..." because what delay to be provided by the corresponding cells are referred to and delay provided by loads, because placement of the selected cells is done after the delay valued determined. The claim is vague because loads are known until after placement because a net (wire) is existed after placement of selected. The claim limitation appears to contradict itself because the determination of delay values is done by information that does not exist.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2, 5 and 7-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kannan et al., "A Methodology and Algorithms for Post-Placement Delay Optimization," ACM, 31st ACM/IEEE Design Automation Conference, 1994, pp. 327-332.

6. As to claim 2, Kannan et al. an automated method for designing an integrated circuit layout with a computer (see entire document), comprising:

(a) selecting a plurality of cells that are intended to be used in the integrated circuit layout (Kannan et al. teach a placement-intelligent resynthesis methodology and optimization algorithms to meet post-layout timing constraints while at the same time reducing interconnect congestion [abstract]; cell libraries [Fig. 6 shows selection of cell to be placed; for example, Fig. 6 describes: "select_suitable.buffer(*L*)"; Fig. 5 show selected buffers p0 and p3 to be placed; Fig. 7 show a plurality of cells in cell libraries are selected for replacement];

(b) determining delay values for corresponding cells in the selected plurality of cells as a a function of delay to be provided by the corresponding cells and delay to be provided by loads on the corresponding cells in order to satisfy delay constraints (section 2 describes placement-based timing analysis including delay calculations of selected cells in order to satisfy delay constraints in placement-based delay optimization described in section 3, by a placement-based synthesis system described in section 4; for example, placement-based delay optimization include insertion of buffers at p0 and p3 in Fig. 5(b) to satisfy delay constraints; the buffer configuration meets the timing constraints as shown in Fig. 5(b), see section 3.1 page 330]; Fig. 5(b) show, for example, buffers p0 and p3 are configurations, in order to meet timing constraints, each of delay values

corresponding to each buffer configurations selected is determined a function of delay to be provided by the corresponding buffers (corresponding to its sizes) and delay to be provided by loads on the corresponding cells (provided loads p4 and p5 for buffer p3; provided loads p2 and p1 for buffer p0; delay value of each of buffer configurations selected to be used in the IC layout must be determined in order to satisfy timing constraints); and

(c) performing a placement of the selected plurality of cells after determining said delay values [Fig. 5(b) show placement of selected buffers at p0 and p3 in order to improve delay after calculation of delay values in section 2], the placement including assigning loads for the selected plurality of cells (Kannan et al. teach placement-based delay optimization including assigning precomputed loads and stored in section 2.1 (for example, precomputed and stored values of loads p1, p2, p4 and p5 shown in Fig. 5(b), in placement shown in Fig. 5(b) and determining a size or area of the selected plurality of cells in response to the said assigned loads and said delay values initial placement [sections 3 and 4 describe placement of buffers at p0 and p3 including assigning loads p1, p2, p4 and p5 that can be precomputed and stored at the nodes described in section 2.1; section 3.2 described gate resizing in order to improve delay to satisfy a number of design and technology constraints]. In addition, Kannan et al. teach the buffer configuration that meets the timing constraints look like the one given in Fig. 5(b), see page 330. The buffer configuration includes characteristics (size or area and delay). In section 3.2, Kannan et al. teach gate resizing. In this teachnique, a cell is replaced with a cell in the library that is equivalent in functionality but having a better drive

strength (determined size or area), intrinsic delay, load or other characteristic that makes it more appropriate [6] (page 330). The entire document applied.

7. As to claim 5, Kannan et al. teach determining the size or area of the cells that will approximately maintain said delay values determined prior to said placement (Fig. 5 and 6 show selected suitable buffers (having determined characteristics including delay and sizes) for placement will improve delay or approximately maintain the delay values). In addition, selected buffer configuration and placed as shown in Fig. 5(b) will meet timing constraints. Also, Kannan et al. teach as a preliminarily step to applying transformations, we strip off all the buffers and merge all redundant inverters introduced by the initial synthesis run. This will allow us to do a placement-based buffer insertion from scratch taking true wire parasitics into account (see section 3, page 329).

8. As to claim 7, Kannan et al. teach routing the digital circuit to generate the integrated circuit layout using a finalized size or area of the selected plurality of cells (section 4 describes a placement based synthesis system and process shown in Fig. 10 and result of IC layout shown in Fig.11 below, where Fig. 11 shows an improved finalized size or area of generated IC layout using finalized size or area of the selected plurality of cells described in section 2-3).

9. As to claim 8, Kannan et al. teach, wherein said delay values are determined using gain (section 2 describes delay computation determined taking consideration of intrinsic gate delay, load delay, interconnect delay and slew sensitivity using gain; these parameters determine a gain of delay values by changing these parameter values).

10. As to claim 9, Kannan et al. teach, wherein said delay values are determined using logical effort (section 2 describes delay values are computed using logical effort, for example, same functionality of gate, by its delay values varied depending on parameter values used for delay calculation).

11. As to claim 10, Kannan et al. teach, wherein said delay values are determined by finding a preferred gain of the cells (section 2 described delays computed by finding a preferred gain of the cells using equation taking intrinsic gate delay, load delay, interconnect delay and slew sensitivity; these parameters are used to find a preferred gain of the cells; for exemple, a buffer configuration selected shown in Fig. 5(b) including size and delay, and of course a gain to satisfy timing constaints described on page 330).

12. As to claim 11, Kannan et al. teach, wherein the preferred gain of the cells is determined using a continuous buffering assumption (Fig. 4 and 5 and show suitable buffers are selected for placement for improving delay, equivalent buffers having continuous of sizes and delay values are determined and stored described in sections 2 and 3).

13. As to claim 12, Kannan et al. teach, wherein said delay values are determined during library analysis (see sections 2-4). Kannan et al. teach selected cells from cell library for placement to meet timing constraints (see section 3).

14. As to claim 13, Kannan et al. teach, wherein said delay values are determined using a typical load of the cells (see section 2). Kannan et al. teach delay calculation based on loads (see section 2).

15. As to claim 14, Kannan et al. teach, wherein the typical load is determined based on gain considerations (section 2). Fig. 5 show a buffer configuration selected based on loads improve delay and meet timing constraints (page 330). Section 2 described delay calculation using various parameters to determine delay values. By changing these parameter values, various delay values are obtained and a gain could be determined. That means a load could be determined based on gain considerations.

16. As to claim 15, Kannan et al. teach, wherein the size or area of the cells is variable and not fixed at the time the cells are selected (section 3 describes gate resizing, therefore selected buffers for placement including variable size or area providing a delay to meet timing constraints).

17. As to claim 16, Kannan et al. an automated method for designing an integrated circuit layout with a computer of a circuit specified by a netlist, comprising:

(a) providing a library of cells (Fig. 6 show component library for cell selection, for example, L is a component library for making selection of buffers or gates or cells; Fig. 8 show Gd library for making selection of buffers or gates or cells for placement or initial placement);

(b) determining initial delay values for a plurality of cells from said library of cells to be used in the integrated circuit layout of the circuit before determining an initial size or area of the cells, and using a timing driven covering method to map said plurality of cells to the circuit (section 2 describes delay computation in placement-based timing analysis; initial delay calculation is performed for a selected cell to be used for placement; for example, Fig. 5(b), a selected buffer having specific buffer configuration

(size, delay) is given for placement for meet timing constraints, see page 330); and (c) performing an initial placement of the cells, including assigning net lengths to nets on the cells, and determining the initial size or area of the cells in response to the initial placement (section 3 describes placement-based delay optimization including gate resizing; section 4 section describes an algorithm in placement-based resynthesis process). Kannan et al. teach: as a preliminarily step applying the transformations see strip off all the buffers and merge all redundant inverters introduced by initial synthesis run. This allow us to do a placement-based insertion from scratch taking true wire parasitics into account. We found that by including buffers in the initial placement, we can minimize changes in the net area of the components in the netlist. This improves chances that the incremental placer will find a solution close to the suggested placement (see section 3 starting page 329).

18. As to claim 17, Kannan et al. teach, inserting buffers based on an estimation of area savings in the circuit prior to determining said initial size or area of the cells (Fig. 5 show selected suitable buffers are inserted at p0 and p3; section 3 describes gate resizing). Section 3.1 describes insertion buffers based on an estimation of area saving in the circuit. Fig. 5(b) show selected suitable buffers for placement and insertion at p0 and p3 and section 3.2 describes gate resizing, that means the insertion of buffers is prior determining initial size or area of the cells because the cells can be resized to fit an assigned die area after layout.

19. As to claim 18, Kannan et al. teach compressing or stretching delay values associated with cells prior to determining said initial delay values for the cells (section 4

describes stripping off all the buffers and removing all redundant cascades introduced by initial synthesis run that will allow do a placement-based buffer insertion taking true wire parasitics into account so that placement-based delay optimization can be done using fanout buffering and gate resizing transformations to reduce delay along critical paths in a network of IC design; section 3 describes that including buffers in initial placement will minimize changes in net area of components in the netlist while minimizing delay, that means stretching delay values).

20. Applicants are requested to consider entire document.

Remarks

21. The claim limitation is vague and imaginary as clearly defined by analysis above. The claim limitations are clearly read on by teachings of the reference. The analysis by applicant is in error because the teachings of Kannan provide post-placement delay optimization. Applicants insist that the delay calculation is done before placement. The amended claim contradicts the actual fact of a circuit design layout because the determination of delay values of selected cells is done within information that does not exist because a delay of loads (net or wire) does not known until placement. A wire is clearly not known until placement. Therefore, the amended claim vague. The claim limitation is still read on Kannan's teachings. Kannan clearly teachings a cell is selected and intended to be used in a circuit layout (Fig. 4 (a) show no buffer is placed (meaning buffer b in Fig. 4(b) is instantly removed); Fig. (b) show a buffer b is selected and intended to be used in the circuit layout; a buffer configuration b is selected (Fig. 6 show that in algorithm; a suitable configuration buffer is selected, meaning that a suitable

configuration must include its size and corresponding delay provided initially before a placement or layout); Fig. (a) and (b) show just an example (Fig. 5 also applied), a delay value of a buffer b is determined taking consideration of its delay provided (initially defined by its size, in the language of a suitable configuration of a buffer is selected) and a delay defined by loads (a net or wire as shown in the connection of Fig. 4 or 5). Kannan's teachings clearly read on the claim limitation. The delay values determined by the claim are based on the fact that does not exist because a wire is known until placement is done. If it a wire is known before placement (but it not true because it is again the actual fact), it appears that claim limitation process is mental process. Kannan's teachings meet the claim limitation because a buffer configuration is selected and intended to be used in a circuit layout as shown in Fig. 4 and 5 and by algorithm shown in Fig. 6 meets the timing constraints as shown in Fig. 5(b). In order to meet such timing constraints the delay values corresponding to configuration of buffers selected to be placed in the circuit layout must be calculated using its delay provided (corresponding to its size(s)) and delay of loads (a net or wire shown as in connection of Fig. 4 and 5). A suitable configuration of buffer selected to meet timing constraint means that a configuration of buffer includes its size and corresponding delay and taking into account associated delay corresponding to loads (a net or wire as shown in the figures 4 and 5). Examiner contends that the delay value determined by Kannan can be done before or after placement. Fig. 4(a) and 5(a) show that inserted cells intended to be used in a circuit layout shown in Fig. 4(b) and 5(b) are determined to meet the timing constraints in post-layout optimization. The fact is whether delay values are determined

before or after placement, the delay values determined are not changed using a methodology and algorithm as taught by Kannan. In addition, a net or wire (loads information is not known before placement). No novelty in the claim limitation what so ever. Fig. 4(a) or 4(b) and Fig. 5(a) o (5b), delay values of buffers intended to be used in the circuit layout does not change but meet the timing constraints. In order to meet the timing constraints, a suitable configuration of buffer selected must be optimized, for example, a size of a gate may be modified, then its delay value must be recalculated based on some metric (it gain) because the reference show a gate is resized and delay is optimized. Examiner sees no novelty in the claim limitations. The claim limitations are clearly taught and suggested by the reference.

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, Art Unit 2825